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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/706,115	11/12/2003	Kevin T. Look	X-1144 US	7705

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EXAMINER	
FULK, STEVEN J	

ART UNIT	PAPER NUMBER
2891	

DATE MAILED: 08/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H·A

Office Action Summary	Application No.	Applicant(s)	
	10/706,115	LOOK, KEVIN T.	
	Examiner	Art Unit	
	Steven J. Fulk	2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17 and 27-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3, 5-17, and 27-30* is/are rejected.

7)☒ Claim(s) *4* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/12/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election of group I, claims 1-17 and 27-30, in the reply filed on July 1, 2005 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1, 5-15, 17, 27-30 are rejected under 35 U.S.C. 102(e) as being anticipated by Kothandaraman '458.

Kothandaraman discloses a non-volatile memory cell comprising a semiconductor body region, a first and second source/drain region coupled to respective first and second contacts, a polysilicon gate electrode and a gate dielectric having a central portion located over a channel region

between the source/drain regions in the body, a third and fourth contact on the first and second ends of the gate electrode where the electrode ends are wider than the central portion, and a fifth contact coupled to the semiconductor body (Fig 4; ¶33, 36-37). The reference also discloses the first and second source/drain regions having a p-type conductivity and the body region comprising an n-type well region (¶40). Kothandaraman discloses first, second, and third control voltages being applied to the gate ends and the semiconductor body region, all of which are less than or equal to normal operating voltages of a CMOS process (¶50). The reference discloses the cell being fabricated using a standard CMOS process (¶33) and comprising current sense circuitry for detecting a read current in the source/drain regions (¶54). Kothandaraman discloses the cell being part of a programmable read-only memory (¶56), being part of a programmable logic device (¶55), or being used to selectively enable or disable a portion of a circuit coupled to the cell (¶5). The reference also discloses a system for enabling a transistor to be operated as a non-volatile memory cell comprising the means to apply a first, positive control voltage and a second, ground control voltage to the ends of a gate electrode, wherein the voltages cause a current to flow through the gate thereby changing the threshold voltage of the transistor (¶17). The system also comprises the means for applying a third program voltage to the body region of the transistor, which

is used to vary the bias on the transistor (¶50). Kothandaraman discloses the system further comprising a means for applying a first read control voltage to the gate electrode and first source/drain region of the transistor, and a means for applying a second read control voltage to the body of the transistor and second source/drain region of the transistor (¶54).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 2 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kothandaraman as described above, and further in view of Hui '670.

Kothandaraman teaches all of the elements of claim 1 and the use of a polysilicon gate electrode, but does not teach the gate electrode comprising a layer of titanium silicide, cobalt silicide, or nickel silicide. Hui teaches the use of a Ti, Co, or Ni silicide over a polysilicon gate of a transistor in a non-volatile memory cell (¶26). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the gate electrode of Hui in the transistor of Kothandaraman, as this is a common practice in

the fabrication of gate electrodes to lower resistance and increase operating speed of the cells.

6. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kothandaraman as described above, and further in view of Rao et al. '582.

Kothandaraman teaches all of the elements of claim 1, but does not teach the use of the non-volatile memory cell to store a portion of an encryption key. Rao does teach the use of a non-volatile memory cell to store a portion of an encryption key (col. 19, lines 20-25). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the memory cell of Kothandaraman to store a portion of an encryption key because encryption keys are conventionally non-volatile memory cells to retain information after a power source is removed, and also because of the high level of security offered due to the logic state of Kothandaraman's cell depending on the transistor channel conductivity which could not easily be deciphered by reverse-engineering of the encryption key.

Allowable Subject Matter

7. Claim 4 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: a search of the relevant art found references disclosing all elements of claims 1 and 2, but did not find the silicide gate of a non-volatile memory cell exhibiting agglomeration to program the cell, as recited in claim 4. Kothandaraman '458 discloses a non-volatile transistor memory that is programmed by running a current through the gate, but the result is a shorted channel as opposed to an open gate. McElroy '836 discloses a read-only memory that is fabricated by printing or not printing gate contacts, resulting in logic 1 or 0 states, but the open gate is not electrically programmable. Hui '670, Li et al. '360, and Szluk et al. 340 disclose a semiconductor non-volatile memory device comprising a transistor and a silicide agglomeration fuse in series, but not comprising a silicide agglomeration gate. Toyoshima '680, Kamiya et al. '200, Kalnitsky et al. '397 and Bohr et al. '700 disclose silicide agglomeration fuse devices, but not in a non-volatile memory cell. Graham et al. '140 and Redfern et al. '839 disclose a programmable read-only memory array wherein the transistor cells are programmed by being made non-conductive, however the programming method comprising opening the source/drain connection of the transistor with a laser as opposed to electrically opening the gate of the transistor.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven J. Fulk whose telephone number is (571) 272-8323. The examiner can normally be reached on Monday through Friday, 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bill Baumeister can be reached on (571) 272-1722. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

sjf
7/29/05

B. WILLIAM BAUMEISTER
SUPERVISORY PATENT EXAMINER